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cont

4 (a) forming a first gate insulating film for forming
5 the MIS transistor structure on a main surface of a
6 semiconductor substrate;

7 (b) forming at least one pair of laminating structure
8 bodies each including two layers of a first gate electrode
9 covering a part of said first gate insulating film and a
10 first insulating film covering said first gate electrode,
11 an etching prevention film being formed on a sidewall
12 portion of said first insulating film but so as not to
13 cover sidewall portions of said first gate electrode;

14 (c) introducing impurities into said semiconductor
15 substrate through said first gate insulating film located
16 in a region not covered with said laminating structure
17 bodies, and thereby forming a first impurity introduced
18 region self-aligned with said laminating structure bodies
19 on the main surface of said semiconductor substrate;

20 (d) removing said first gate insulating film in the
21 region not covered with said laminating structure bodies
22 after said step (c); and

23 (e) forming a second insulating film covering upper
24 portions and sidewall portions of said laminating structure
25 bodies after said step (d).

B9
cm 1 9. 15. (Amended) A method for manufacturing a
2 semiconductor integrated circuit device, comprising the
3 steps of:

4 (a) forming, on a main surface of a semiconductor
5 substrate, a first gate insulating film consisting of a
6 silicon oxide film, and forming a first conductive film, a
7 second gate insulating film and a second conductive film
8 over said first gate insulating film in this order:

9 (b) forming a first protection insulating film
10 consisting of a single layer silicon oxide film formed over
11 said second conductive film, with or without a laminating
12 silicon nitride film formed over the silicon oxide film;

13 (c) patterning said first protection insulating film,
14 and thereby forming an etching mask consisting of said
15 first protection insulating film;

16 (d) patterning said second conductive film, said
17 second gate insulating film and said first conductive film
18 in this order by dry etching using said etching mask as a
19 mask, and thereby forming a plurality of gate electrodes
20 that each have a floating gate electrode formed by a
21 portion of said first conductive film and a control gate
22 electrode formed by a portion of said second conductive
23 film and that each have a laminating structure in which an

B4
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24 upper portion of said control gate electrode is covered
25 with said first protection insulating film;

26 (e) forming an etching prevention film consisting of
27 a silicon nitride film on the patterned first protection
28 insulating film, after said step (c) and before said step
29 (d), or after said step (d), said etching prevention film
30 being formed on both sidewall portions of the patterned
31 first protection insulating film but so as not to cover
32 sidewall portions of said floating gate electrode and said
33 control gate electrode formed in said step (d);

34 (f) introducing impurities into the main surface of
35 said semiconductor substrate located between sidewall
36 portions facing each other in said plurality of gate
37 electrodes, and thereby forming a source region and a drain
38 region;

39 (g) treating a surface of said semiconductor
40 substrate by using etchant containing a hydrofluoric acid
41 after said step (f), and thereby cleaning said first gate
42 insulating film located between the sidewall portions which
43 face each other in said plurality of gate electrodes;

44 (h) covering an upper portion and both sidewall
45 portions of each of said plurality of gate electrodes after
46 said step (g), and forming a second protection insulating

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Cont. 47 film consisting of a silicon nitride film having such a
48 thickness as to partially embed a region between the
49 sidewall portions which face each other in said plurality
50 of gate electrodes;

51 (i) forming, on an upper portion of said second
52 protection insulating film, an interlayer insulating film
53 consisting of a silicon oxide film, and embedding, with
54 said interlayer insulating film, the region between the
55 sidewall portions which face each other in said plurality
56 of gate electrodes;

57 (j) etching said interlayer insulating film and said
58 second protection insulating film located between the
59 sidewall portions which face each other in said plurality
60 of gate electrodes, and thereby forming a first connection
61 hole for exposing a surface of said source region and a
62 second connection hole for exposing a surface of said drain
63 region; and

64 (k) forming a third conductive film electrically
65 connected to said source region inside said first
66 connection hole, and forming a fourth conductive film
67 electrically connected to said drain region inside said
68 second connection hole.

B5
cont.

11.
~~21.~~ (Amended) The method for manufacturing a
semiconductor integrated circuit device according to claim
10
~~20,~~
wherein each of said plurality of gate electrodes
constitutes part of a respective memory cell of a flash
memory, and writing into said memory cell is carried out by
injecting a charge into said floating gate electrode
thereof, and erasing from said memory cell is carried out
by discharging, to said semiconductor substrate, said
charge injected into said floating gate electrode thereof.

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Please add the following new claims:

B6

15.
~~25.~~ (New) The method for manufacturing a
semiconductor integrated circuit device according to claim
9
~~10,~~
wherein said step (g) is conducted so that said first
gate insulating film retreats beneath opposite sidewall
portions of said floating gate electrode.

16.
~~26.~~ (New) A method for manufacturing a semiconductor
integrated circuit device having an MIS transistor
structure of a flash memory, comprising the steps of:

B6

4 (a) forming, on a main surface of a semiconductor
5 substrate, a first gate insulating film, and forming a
6 first conductive film, a second gate insulating film and a
7 second conductive film over said first gate insulating film
8 in this order;

9 (b) forming a first protection insulating film
10 consisting of a single layer silicon oxide film formed over
11 said second conductive film, with or without a laminating
12 silicon nitride film formed over the silicon oxide film;

13 (c) patterning said first protection insulating film,
14 and thereby forming an etching mask consisting of said
15 first protection insulating film;

16 (d) patterning said second conductive film, said
17 second gate insulating film and said first conductive film
18 in this order by dry etching using said etching mask as a
19 mask, and thereby forming a plurality of gate electrodes
20 that each have a floating gate electrode formed by a
21 portion of said first conductive film and a control gate
22 electrode formed by a portion of said second conductive
23 film and that each have a laminating structure in which an
24 upper portion of said control gate electrode is covered
25 with said first protection insulating film;

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26 (e) forming an etching prevention film consisting of
27 a silicon nitride film on the patterned first protection
28 insulating film, after said step (c) and before said step
29 (d), or after said step (d), said etching prevention film
30 being formed on both sidewall portions of the patterned
31 first protection insulating film but so as not to cover
32 sidewall portions of said floating gate electrode and said
33 control gate electrode formed in said step (d);

34 (f) introducing impurities into the main surface of
35 said semiconductor substrate located between sidewall
36 portions facing each other in said plurality of gate
37 electrodes, and thereby forming a source region and a drain
38 region;

39 (g) treating a surface of said semiconductor
40 substrate by using etchant after said step (f);

41 (h) covering an upper portion and both sidewall
42 portions of each of said plurality of gate electrodes after
43 said step (g), and forming a second protection insulating
44 film consisting of a silicon nitride film having such a
45 thickness as to partially embed a region between the
46 sidewall portions which face each other in said plurality
47 of gate electrodes;

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86

48 (i) forming, on an upper portion of said second
49 protection insulating film, an interlayer insulating film
50 consisting of a silicon oxide film, and embedding, with
51 said interlayer insulating film, the region between the
52 sidewall portions which face each other in said plurality
53 of gate electrodes;

54 (j) etching said interlayer insulating film and said
55 second protection insulating film located between the
56 sidewall portions which face each other in said plurality
57 of gate electrodes, and thereby forming a first connection
58 hole for exposing a surface of said source region and a
59 second connection hole for exposing a surface of said drain
60 region.

1 ^{17.}
~~27.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹⁶
~~26,~~ further comprising the steps of:

4 (k) forming a third conductive film electrically
5 connected to said source region inside said first
6 connection hole, and forming a fourth conductive film
7 electrically connected to said drain region inside said
8 second connection hole.

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~~28.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹⁷
~~27,~~
4 wherein said third conductive film formed inside said
5 first connection hole functions as a part of a source line,
6 and said fourth conductive film formed inside said second
7 connection hole functions as a part of a data line.

1 ^{19.}
~~29.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹⁸
~~28,~~
4 wherein each of said plurality of gate electrodes
5 constitutes part of a respective memory cell of a flash
6 memory, and writing into said memory cell is carried out by
7 injecting a charge into said floating gate electrode
8 thereof, and erasing from said memory cell is carried out
9 by discharging, to said semiconductor substrate, said
10 charge injected into said floating gate electrode thereof.

1 ^{20.}
~~30.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹⁶
~~26,~~
4 wherein said flash memory is a NOR type flash memory.

06 1 ^{21.}
~~31.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹⁶
~~26,~~
4 wherein said step (g) is conducted so that said first
5 gate insulating film retreats beneath opposite sidewall
6 portions of said floating gate electrode.

1 ^{22.}
~~32.~~ (New) The method for manufacturing a
2 semiconductor integrated circuit device according to claim
3 ¹
~~11,~~
4 wherein said step (d) is conducted such that said
5 first gate insulating film retreats beneath opposite
6 sidewall portions of said first gate electrode.
